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A Reduced Devices for 9-level Multi-level inverter with different Modulation techniques using Reversing Voltage Topology

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ABSTRACT
Use of multilevel inverters has become popular in recent years for high-power high-voltage applications and their performance is better to that of conventional two-level inverters due to higher number of dc voltage sources, reduced harmonic distortion and lower EMI. Various topologies and modulation strategies have been investigated for utility and drive applications in this paper. This paper proposed a new multi-level inverter topology is called Reversing Voltage with Phase opposition disposition PWM technique. A proposed carrier based pulse-width modulation strategy for multi-level inverter topology is used to produce nine-level output voltage in single-phase and it also requires less number of components as compared to other multi-level inverter topologies. However, multi-level inverter has some disadvantages such as increased number of components, complex pulse-width modulation controlling method, and voltage-balancing problem. Finally simulation result of a new multi-level inverter topology is presented with phase opposition disposition PWM technique in single-phase nine-level.

Keywords—Multi-level inverter, RV topology and PWM technique.

I. INTRODUCTION

In recent years multi-level inverters have been widely available for high-power high-voltage applications such as uninterruptible power supplies, flexible ac transmission systems, and HVDC. Where as conventional two-level inverter have some limitations in high-power high-voltage applications due to switching losses and power ratings [1-2]. Basically this power conversion is provided more than two voltage levels to achieve smoother and less distorted dc to ac power conversion. A desired output voltage waveform can be synthesized from the multiple voltage levels with less distortion, less switching frequency and higher efficiency. To obtain a quality output voltage waveform they require high switching frequency along with different pulse-width modulation strategies [3]. Advantages of multi-level inverter when compared with the conventional inverter; improves the output voltage waveform, reduced voltage stress on the load and also decreases electromagnetic interference problems, and it has some disadvantages such as complex PWM controlling method, voltage balancing problem and it requires higher number of semiconductor switches. Lower voltage rated switches can be used in multi-level inverter instead of higher number of semiconductor switches which minimizes cost of the semiconductor switches as compared to two level inverters [4].

An equivalent representation of one phase leg of inverters with different levels shown in figure 1, and power semiconductors is represented by an ideal switch with several positions [3].

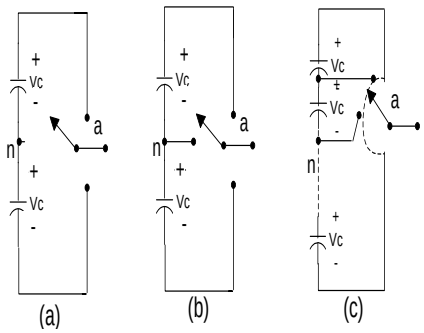

Fig. 1 one phase leg of inverter (a) two level (b) three level (c) n-levels

In particular, multilevel inverters allow the operation at higher dc voltages using semiconductor switches connected in series and produce voltage waveforms with better harmonic profile than conventional two-level inverters [5]. There are three main topologies of multilevel inverters: neutral point-clamped, flying capacitors (capacitor clamped), and cascaded H-bridge. In 1981 Nabae introduced a three level diode clamped inverter schemes [6]. In neutral-point-clamped inverter the dc-link is separate into number of smaller voltage levels using a bank of series connected bulk capacitors. The series-connected H-bridge topology of multilevel inverters has been used for induction motor drives and it requires separate DC supply for all three phases, which increases the power circuit complexity [7].

In this paper a new multilevel inverter topology is proposed is called Reversing Voltage (RV). The Reversing Voltage topology that was previously proposed [8] here is implemented in single-phase nine-level inverter with phase opposition disposition PWM. A Phase opposition disposition PWM scheme offers great advantages such as improved output voltage waveforms, lower EMI, and lower THD in comparison of other PWM switching schemes. Particularly at higher levels this topology requires less number of components as compared to two-level inverters [8].

II. PROPOSED TOPOLOGY

The block diagram of multi-level inverter using Reversing Voltage topology is shown in fig. 2.1. The principle idea is that, the left side circuit generates the required positive level is called positive level generator and the right side circuit is called full bridge converter which reverses the voltage direction when the voltage polarity requires to be changed for negative polarity (negative half cycle of the fundamental output voltage) [6].

This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is called level generation part and is responsible for level generating in positive polarity. The other part is called polarity generation part and is responsible for generating the polarity of the output voltage. The level generation part requires high-frequency switches to generate the required levels while polarity generation part requires low-frequency switches which is the low-frequency part operating at line frequency [7]. This topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. The positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. It requires ten switches and three isolated dc sources.

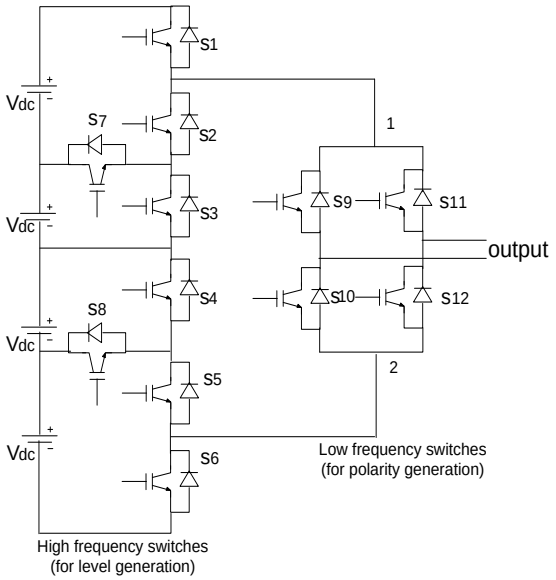

Figure 2.1. Single-phase nine-level inverter for R-L load.

The proposed topology is a symmetrical topology since all the values of all voltage sources are equal and it does not face voltage-balancing problems due to fixed dc voltage values. It is easily extends to higher voltage levels by duplicating the middle stage as shown in Fig. 3 [9].

The primary objective of this paper is to minimize the total harmonic distortion of 9-level inverter with phase opposition disposition PWM scheme as compared to other PWM schemes. It also minimizes power semiconductor switches than conventional multilevel inverter. For a single-phase 9-level multi-level inverter model, there are 16 switches are needed, whereas the proposed model uses only 12 switches. The operation of the proposed topology has been discussed in detail and has been verified with the help of Matlab/ simulations [10].

III. MODES AND ITS OPERATION

The operation of this topology can be easily understood by mode of operation of single-phase nine-level inverter shown in fig. 2.2. There are nine sufficient switching modes in generating the multistep level for a nine-level inverter.

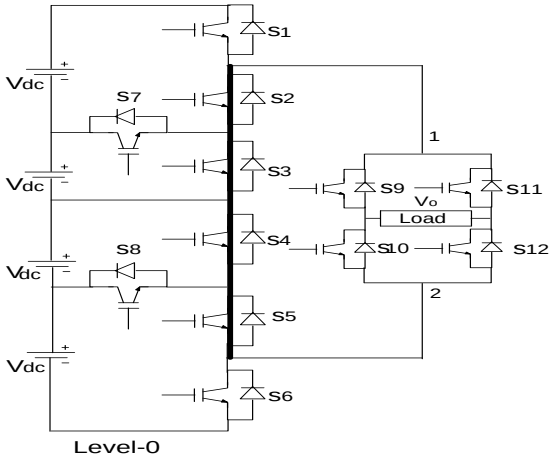

Fig. (a)

The output voltage will be zero (i.e., level 0) When switches S2, S3, S4 and S5 are turned "on" shown in fig. (a).

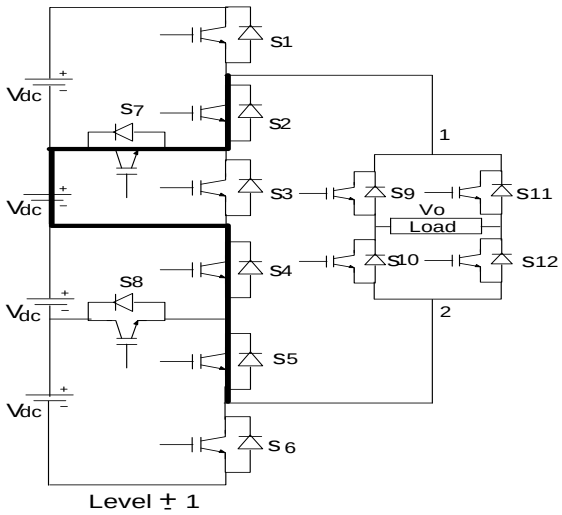

Fig. (b)

When switches S2, S4, S5 and S7 are turned "on" the output voltage will be "Vdc" (i.e., level 1) shown in fig. (b).

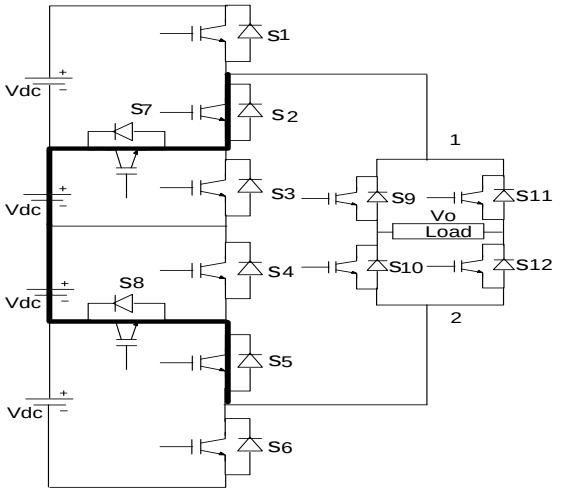

Fig. (c)

When switches S2, S5, S7 and S8 are turned "on" the output voltage will be "2Vdc" (i.e., level 2) shown in fig. (c).

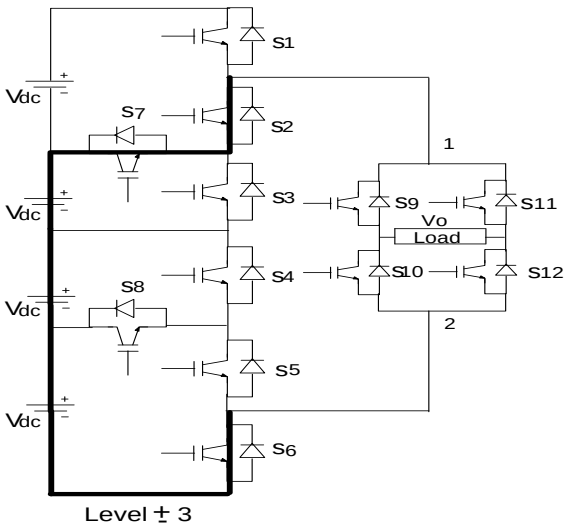

Fig. (d)

TABLE-I Switching scheme for 9-level inverter

LEVEL	SWITCH STATES												OUTPUT VOLTAGE
	S1	*S2*	*S3*	*S4*	*S5*	*S6*	*S7*	*S8*	*S9*	*S10*	*S11*	*S12*	
4	✓					✓				✓	✓		4Vdc
3		✓				✓	✓			✓	✓		3Vdc
2		✓			✓		✓	✓		✓	✓		2Vdc
1		✓		✓	✓		✓			✓	✓		Vdc
0		✓	✓	✓	✓				✓	✓	✓	✓	0
-1		✓		✓	✓		✓		✓			✓	-Vdc
-2		✓			✓		✓	✓	✓			✓	-2Vdc
-3		✓				✓	✓		✓			✓	-3Vdc
-4	✓					✓			✓			✓	- 4Vdc

When S2, S6 and S7 switches are turned "on" the output voltage will be "3Vdc" (i.e., level 3) shown in fig. (d).

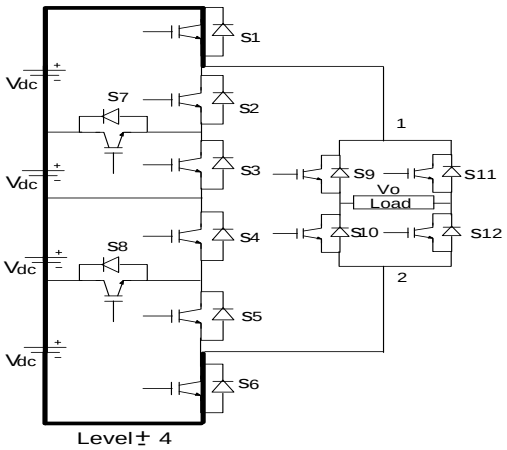

Fig. (e)

Figure 2.2: fig (a), fig (b), fig (c), fig (d), fig (e) are Switching combinations of multi-level inverter topology for different level.

When switches S1 and S6 are turned on the output voltage will be "4Vdc" (i.e., level 4).

Switches S9, S10, S11 and S12 are used to reverse the voltage direction when polarity requires to be changed. When switches S10 and S11 are turned "on" together positive half cycle will be generated and when S9 and S12 are turned "on" together negative half cycle will be generated across the load. The voltage blocking capacity of each switch is Vdc [2]. Each voltage source "Vdc" is required 100V. According to the table, there are nine switching combinations to control the multi-level inverter and it shows the great redundancy of the switching devices. Operation of the single-phase nine-level inverter with reversing voltage topology can be easily explained with the help of fig. 2.2 and Table I

IV. MODULATION TECHNIQUES

There are different pulse width modulation strategies with different phase relationships.

- Phase disposition pulse width modulation (PD PWM):- In phase disposition pulse width modulation strategy, where all carrier waveforms are in same phase.
- Phase opposition disposition pulse width modulation (POD PWM):- In phase opposition disposition pulse width modulation strategy, where all carrier waveforms above zero reference are in phase and below zero reference are 180^0 out of phase.
- Alternate phase opposition disposition pulse width modulation (APOD PWM):- In alternate phase opposition disposition PWM scheme where every carrier waveform is in out of phase with its neighbor carrier by 180^0.

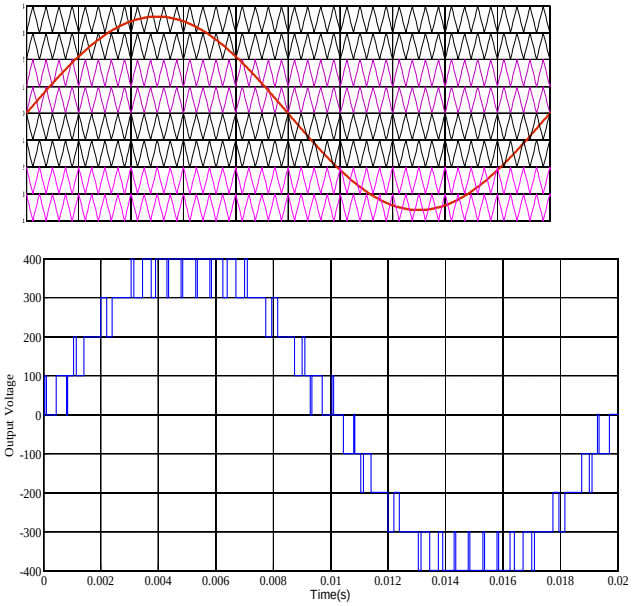

Figure 3.1: POD PWM Scheme and nine-level output voltage.

In Fig. 3.1 for N-level inverters there are N-1 triangle carriers are used and which is compared by the sinusoidal waveform. Whenever sinusoidal waveform is greater than carriers then gating signals are generate.

V. SIMULATION RESULTS:

In this section a simulation model of Reversing Voltage topology for a single-phase nine-level inverter is implemented. The simulation parameters are as following R = 20 ohms, L = 10mH, dc source voltage is 400V; Frequency of carrier signal is 2 kHz. In this topology, phase opposition disposition PWM scheme is used. Table II shows THD for different PWM switching schemes with different modulation index.

TABLE-II
PERCENTAGE THD FOR DIFFERENT PWM STRATEGIES.

Modulation Index	PD PWM % THD	POD PWM % THD	APOD PWM % THD
1.1	12.45	11.73	13.19
1	14.20	13.70	14.43
0.9	16.94	16.84	16.94

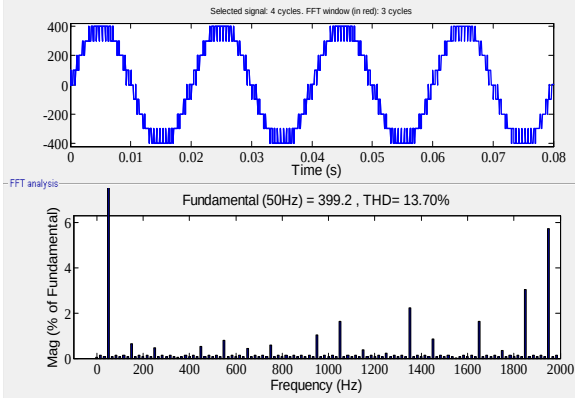

Figure 4.1 POD PWM output voltage and harmonic spectrum (Modulation index 1.0)

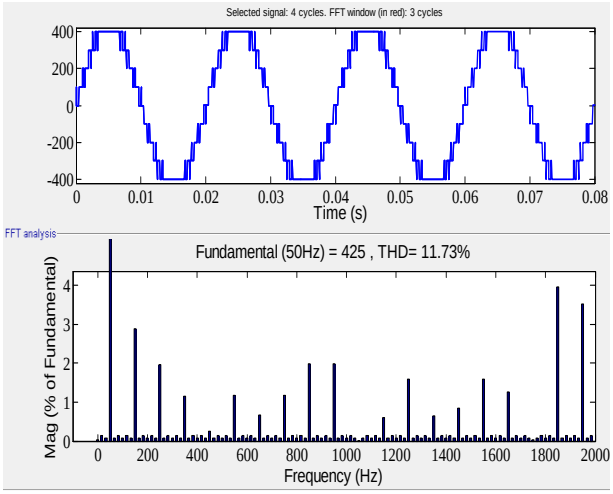

Figure 4.2: POD PWM output voltage and harmonic spectrum (Modulation index 1.1)

The number of required components for single-phase nine- level inverter is shown in Table III.

TABLE-III
Comparison between different multilevel inverter topologies

Inverter type	NPC	Flying capacitor	cascade	Proposed
Main switches	2(N-1)	2(N-1)	2(N-1)	(N-1)+4
Main diodes	2(N-1)	2(N-1)	2(N-1)	(N-1)+4
Clamping diodes	2(N-2)(N-1)	0	0	0
DC bus Capacitor/ Isolated supplies	(N-1)	(N-1)	3(N-1)/2	(N-1)/2
Flying capacitors	0	(N-1)(N-2)/2	0	0
Total numbers	(N-1)(2N+1)	(N-1)(N+8)/2	11/2(N-1)	(5N+11)/2

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CONCLUSION:

In this paper, a new multi-level inverter topology with phase opposition disposition pulse width modulation is proposed. Reversing Voltage topology with phase opposition disposition PWM technique is used to produce nine level output voltage in single-phase and minimize total harmonic distortion as compared to other PWM techniques. This multi-level inverter topology improves output voltage, reduces higher number of semiconductor switches and voltage stress on semiconductors switches and it also requires less number of components compared to two level inverter. One of the most advantages of the topology is that it requires less high-switching-frequency components. Simulation results show the performance of single-phase nine-level inverter with improved THD.

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